REMARKS

This paper responds to the Office Action dated on October 31, 2007.

No claims are amended, no claims are canceled, and no claims are added; as a result, claims 1-2, 6-10, 14-15, 19-23, 27-31, 35-37, 51-52, 54-56 and 62 are now pending in this application.

§*103 Rejection of the Claims*

Claims 1, 2, 6, 7, 14, 15, 19, 20, 51, 52, 56 and 62 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Ma et al. (U.S. Patent No. 6,207,589) in view of Park (U.S. Patent No. 5,795,808) and Yano et al. (U.S. Patent No. 5,810,923). Applicant respectfully traverses this rejection.

Ma teaches the benefits of ***heavily*** doped deposition of a metal layer to be oxidized to form the gate dielectric of a transistor. Applicant emphatically disagrees with the Examiner's repeatedly ignoring the extremely clear teaching of the cited reference, as seen on page 16, second paragraph of the outstanding Office Action. Ma teaches the deposition of Zr or Hf mixed with up to 50% of a trivalent metal such as aluminum, with 25% being taught as the preferred level. This teaching of the importance of the use of extremely impure metal is repeated everywhere throughout the cited reference, starting with the abstract saying that the doping with trivalent materials causes the film to "resist the formation of a crystalline structure, interfaces to adjacent films have fewer irregularities", and "the film can be made thin to support smaller transistor geometries, while the surface of the channel region can be made smooth to support high electron mobility". The figures show the properties, such as IV characteristics, leakage currents, time dependent dielectric breakdown voltages, and time to failure plots, of trivalent doped metals, but nothing of pure metals. The benefits of the amorphous (i.e., non crystalline) nature of the alloyed or doped dielectric film formed by 25 to 50% trivalent metal in the film is discussed at least in col. 1, lines 35, 41, 53, 60, 64; col. 2, lines 2, 21, 24, 27, 29, 37, 39, 43, 49, 61, 68; col. 3, lines 3, 13, 34, 36, 45, 50, 61, 63; col. 4, lines 1, 5, 14, 20, 21, 28, 29, 46, 57, 64; col. 5, lines 44, 53, 62, 65 (listing the range of 0-50%); col. 6, lines 21, 23, 26, 34, 42, 46, 51, 60; col. 7, lines 6, 9, 11, 17, 21, 22, 31, 47, 65; col. 8, lines 20, 25, 27, 31, 37, 56, 61, 67; col. 9, lines

6, 8, 13, 17; and col. 10, line 18. Applicant respectfully submits that essentially the entire teaching of Ma is towards heavily doped metals.

The test for obviousness under 35 USC § 103 must take into consideration the invention as a whole. *Interconnect Planning Corp. v. Feil*, 774 F.2d 1132, 1143, 227 U.S.P.Q. 543, 551 (Fed. Cir. 1985). The Examiner must also recognize and consider not only the similarities but also the critical difference between the claimed invention and the prior art. *In re Bond*, 910 F.2d 831, 834, 15 U.S.P.Q.2d (BNA) 1566, 1568 (Fed. Cir. 1990) *reh'g denied,* 1990 U.S. App. LEXIS 19971 (Fed. Cir. 1990). Applicant respectfully submits that taken as a whole the critical difference includes that Ma has a discussion in virtually every paragraph teaching the benefit of heavy addition of trivalent metal in the taught metals of zirconium and hafnium, while the present claimed invention specifies that the metal is very pure.

Ma teaches that it "would be advantageous if improved high-k dielectric materials could be formed by simply doping ... additional elements" (col. 2, lines 58-62) to existing high-k elements. One of ordinary skill in the art would understand Ma to be teaching doping a high-k dielectric with heavy amounts of another material to prevent "the formation of an interfacial SiO_2 layer" (col. 1 lines 45-47) by the addition of a "trivalent metal" (col. 2, lines 1-3) not to exceed 50% (col. 2, lines 1-3). One of ordinary skill in the art would not understand Ma to teach the use of pure metals, which are never mentioned in the cited reference. The present application discusses using pure metal with a purity of 0.999999 at page 7 line 8.

Ma discloses an interface barrier 62 of 2-5 Å of silicon nitride or silicon oxynitride (col. 2, lines 11-17; col. 6, lines 4-11 and figures 12 and 13), and the existence of "an interfacial SiO_2 layer" (col. 1 lines 45-47). Ma suggests the intentional use of interface barrier 62 to prevent increase in the interfacial layer. Ma does not teach or suggest direct contact of dielectric to the channel region.

Park is used to show that sputtering and evaporation are art recognized equivalents (see outstanding Office Action on page 3, fourth paragraph). Applicant objects to this and submits that the present application teaches why the use of sputtering may cause the rough surface and crystal damage shown in the present application's figure 2b and discussed at least on page 3, lines 17-23 and page 7, line 22. This damage is discussed on page 3, line 1 as increasing the leakage current through the gate oxide by a factor of ten times for each 0.1 nm increase in

roughness. The present specification (page 6, lines 9-18, and page 7, line 20) contrasts the use of a thermal evaporation technique for smooth surfaces and minimal unwanted silicides and oxides to improve the surface smoothness, while the cited references fail to mention anything with regard to these issues.

Yano is used to show that the deposition of a pure metal, the oxidation of metal, and that smooth metal oxide surfaces are known. Yano teaches the deposition of an oxide film from an alloy of metals having up to 75% of a rare earth metal (col. 8, line 33) in a vacuum chamber with an oxidizing gas (col. 8, line 57) to form an epitaxial oxide layer, which is by definition not amorphous. Yano teaches only crystalline dielectrics and uses the term epitaxial repeatedly throughout the entire specification. One of ordinary skill in the art would easily understand the definition of epitaxial to mean not only crystalline, but single crystalline material with a specific orientation. Yano teaches against amorphous materials, pure metals, and the direct contact of the dielectric to the semiconductor material.

Specifically, Applicant respectfully submits that the suggested combination of Ma with Park and Yano fails to describe or suggest at least the claimed feature of a "*...evaporation depositing a substantially amorphous and 0.99999 pure single element metal layer directly contacting a single crystal semiconductor portion of the body region using electron beam evaporation at a temperature between 150 to 200 °C...*", as recited in independent claim 1. The other independent claims recite similar limitations. The combination of cited references, whether taken alone or in any combination, do not suggest the use of pure metal deposition, or the use of thermal evaporation as compared to sputtering, or directly contacting the semiconductor body region with the dielectric layer.

The dependent claims are held to be patentable at least as depending from patentable base claims as shown above, since any claim depending from a nonobvious independent claim is also nonobvious. See M.P.E.P. § 2143.03. In view of the failure of the suggested combination of references to describe or suggest pure metal, amorphous oxide, or direct contact between the oxide and the substrate, Applicant requests this rejection under 35 U.S.C. § 103(a) be reconsidered and withdrawn.

Claims 8-10, 21 and 54 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Ma et al. (U.S. Patent No. 6,207,589) in view of Park (U.S. Patent No. 5,795,808) and Yano et al. (U.S. Patent No. 5,810,923) as applied to claims 1, 2, 6, 7, 14, 15, 19, 20, 51, 52, 56 and 62 above, and further in view of Moise et al. (U.S. Patent No. 6,211,035). Applicant respectfully traverses this rejection.

The cited references of Ma, Yano and Park have features discussed above. Moise is used to show that annealing in an inert ambient such as krypton, and in conjunction with the oxidizing anneal of Ma are known.

Applicant respectfully submits that the suggested combination of references fails to describe or suggest at least the claimed feature of a "*...evaporation depositing a substantially amorphous and 0.99999 pure single element metal layer directly contacting a single crystal semiconductor portion of the body region using electron beam evaporation at a temperature between 150 to 200 °C...*", as recited in independent claim 1, with similar wording in independent claims 9 and 51, from which the claims in question depend. The reasons are similar to those given above and previously.

The dependent claims are held to be patentable at least as depending from patentable base claims as shown above, since any claim depending from a nonobvious independent claim is also nonobvious. See M.P.E.P. § 2143.03. In view of the failure of the suggested combination of references to describe or suggest the above noted features, Applicant requests this rejection under 35 U.S.C. § 103(a) be withdrawn.

Claims 22, 23, 25, 27, 28, 30, 31, 33, 35 and 36 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Ma et al. (U.S. Patent No. 6,207,589) in view of Park (U.S. Patent No. 5,795,808) and Yano et al. (U.S. Patent No. 5,810,923) as applied to claims 1, 2, 6, 7, 14, 15, 19, 20, 51, 52, 56 and 62 above, and further in view of Maiti et al. (U.S. Patent No. 6,020,024) and in view of the admitted prior art (pages 1-4). Applicant respectfully traverses this rejection.

The cited references of Ma, Yano and Park are discussed above. Maiti is used to show that transistors formed of a metal oxide with a high-k gate dielectric are known in the art.

Applicant respectfully submits that the suggested combination of references fails to describe or suggest at least the claimed feature of a "*...evaporation depositing a substantially*

amorphous and 0.99999 pure single element metal layer directly contacting the body region...;oxidizing the metal layer to form a metal oxide layer directly contacting the body region, wherein the metal oxide layer is amorphous and has a smooth surface...", as recited in independent claim 22. The reasons are similar to those given above and previously.

The dependent claims are held to be patentable at least as depending from patentable base claims as shown above, since any claim depending from a nonobvious independent claim is also nonobvious. See M.P.E.P. § 2143.03. In view of the failure of the suggested combination of references to describe or suggest either thermal evaporation of pure metal, oxidation of the metal to form an amorphous oxide, or direct contact between the oxide and the semiconductor substrate, Applicant requests this rejection under 35 U.S.C. § 103(a) be withdrawn.

Claims 29 and 37 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Ma et al. (U.S. Patent No. 6,207,589) in view of Park (U.S. Patent No. 5,795,808), Yano et al. (U.S. Patent No. 5,810,923), Maiti et al. (U.S. Patent No. 6,020,024), and the admitted prior art, as applied to claims 22, 23, 25, 27, 28, 30, 31, 33, 35 and 36 above, and further in view of Moise et al. (U.S. Patent No. 6,211,035). Applicant respectfully traverses this rejection.

The cited references have all been discussed above, and do not describe or suggest at least the claimed feature of "*...evaporation depositing a substantially amorphous and 0.99999 pure single element metal layer directly contacting the body region using electron beam evaporation... the metal being chosen from the group IVB elements of the periodic table; oxidizing the metal layer to form a metal oxide layer directly contacting the body region, wherein the metal oxide layer is amorphous and has a smooth surface ...*", as recited in independent claims 22 and 30. Claims 29 and 37 depend from claims 22 and 30 respectively. The reasons are similar to those given above and previously.

The dependent claims are held to be patentable at least as depending from patentable base claims as shown above, since any claim depending from a nonobvious independent claim is also nonobvious. See M.P.E.P. § 2143.03. In view of the failure of the suggested combination of references to describe or suggest either thermal evaporation of pure metal, oxidation of the metal to form an amorphous oxide, or direct contact between the oxide and the semiconductor substrate, Applicant requests this rejection under 35 U.S.C. § 103(a) be withdrawn.

Reservation of Rights

In the interest of clarity and brevity, Applicant may not have equally addressed every assertion made in the Office Action, however, this does not constitute any admission or acquiescence. Applicant reserves all rights not exercised in connection with this response, such as the right to challenge or rebut any tacit or explicit characterization of any reference or of any of the present claims, the right to challenge or rebut any asserted factual or legal basis of any of the rejections, the right to swear behind any cited reference such as provided under 37 C.F.R. § 1.131 or otherwise, or the right to assert co-ownership of any cited reference. Applicant does not admit that any of the cited references or any other references of record are relevant to the present claims, or that they constitute prior art. To the extent that any rejection or assertion is based upon the Examiner's personal knowledge, rather than any objective evidence of record as manifested by a cited prior art reference, Applicant timely objects to such reliance on Official Notice, and reserves all rights to request that the Examiner provide a reference or affidavit in support of such assertion, as required by MPEP § 2144.03. Applicant reserves all rights to pursue any cancelled claims in a subsequent patent application claiming the benefit of priority of the present patent application, and to request rejoinder of any withdrawn claim, as required by MPEP § 821.04.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance, and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney David Suhl at (508) 865-8211, or the undersigned attorney at (612) 349-9587 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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Date 31 Jan '08 By _____

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop Amendment, Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this 31 day of January 2008.

Lisa Rossiter _____ _____

Name Signature